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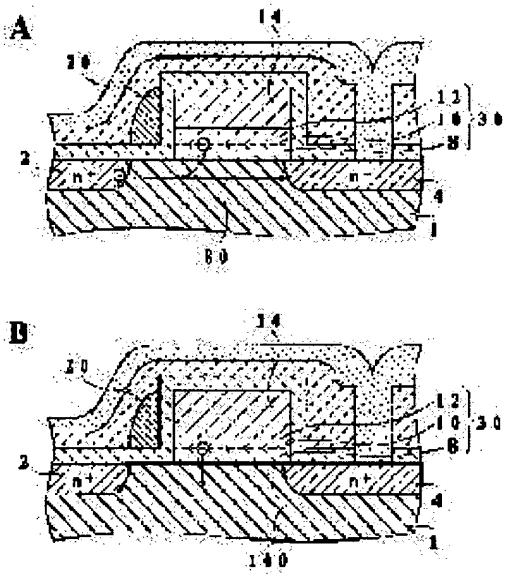
(54) SEMICONDUCTOR DEVICE

(57)Abstract:

PURPOSE: To provide a semiconductor device with which a read-out operation can be conducted accurately.

CONSTITUTION: When a write operation is conducted, high voltage is applied to a source 2, and a channel 8 is formed by electrons jumped out to a drain 4 from the source 2. When low voltage is applied to a selection gate 20, an electric field is concentrated between a selection gate 14 and a substrate 1, a part of electrons are turned to hot electrons, and it is attracted toward a control gate 14 where high voltage is applied. The attracted hot electrons are trapped to the side of the source 2 of a nitrogen film 10, and information is written. When a read operation is conducted, a depletion layer 100 is spread in the vicinity of a drain 4 by the application of high voltage, but does not reach the point where information is written. Accordingly, whether electrons are trapped (information is written) by the nitrogen film 10 can be detected accurately.



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[Date of extinction of right]	

* NOTICES *

CLAIMS

[Claim(s)]
[Claim 1] The semiconductor device by which it characterizes [having-side conductive layer which insulated with field which can be cable run formed, was prepared on / by the side of the control electrode prepared on the trap film which was prepared in the source field prepared in a substrate, and a substrate, and be prepared so that the field which can be cable run formed may form a source field and in between, and be prepared on / which can be drain field cable run formed / a field, and the trap film, and the source / which can be cable run formed / field, insulated with control electrode on side face of control electrode, and was prepared in it].

[Translation done.]

* NOTICES *

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to read-out of the data of a semiconductor device. It is especially related with accuracy-ization of read-out.
[0002]
[Description of the Prior Art] Generally, as trap film of trap mold semiconductor memory, the ONO film (Oxide-Nitride-Oxide) film is used. O film of this ONO film is an oxide film, and an insulator layer. On the other hand, N film is a nitride and is electric conduction film. In addition, N film which is electric conduction film is inserted into O layers which are oxide films. In the case of writing, an electron is led to this N film.
[0003] The sectional view of the trap mold memory which used the ONO film for drawing 9 A and 9B is hung up, and the writing and elimination of data are shown and explained. The source 2 and a drain 4 are formed in the substrate 1 at the trap mold memory 200. The ONO film (the [1O film 8, the N (nitriding) film 10, and] 2O film 12) is formed between this source 2 and a drain 4, and the control gate 14 is formed in that upper part.
[0004] The outline of the write-in principle of this trap mold memory 200 is explained using drawing 9 A. At the time of writing, a channel is formed by an electron being emitted to a drain 4 from the source 2. The trap of a part of this emitted electron is carried out to the N (nitriding) film 10 near the drain as a hot electron. If the trap of the electron is carried out to the N (nitriding) film 10, the threshold electrical potential difference of control gate voltage required in order to form a channel will become large. Thus, it is called the condition that the condition that the threshold became large was written in "1." On the other hand, the trap of the electron is not carried out but it is called the condition that the condition that a threshold is still small is written in "0."
[0005] On the other hand, in elimination, it is impressing a negative electrical potential difference to the control gate 14, and impressing a forward electrical potential difference to a drain, and the negative electron which led the electron hole to N film and was poured into it is neutralized (refer to drawing 9 B). In addition, read-out can read that "1" is written in, if a sense electrical potential difference (mean value in case a trap is not carried out to a threshold electrical potential difference in case the trap of the electron is carried out) is impressed to the control gate and a channel is not formed. Moreover, if a channel is formed, what (it is "0") "1" is not written in for can be read. Thus, in trap mold memory, writing, elimination, and read-out of "1" can be performed free.
[0006]
[Problem(s) to be Solved by the Invention] However, there were the following problems in the conventional trap mold memory. With conventional equipment, as explained using drawing 9 A, the trap of the electron was carried out to the drain 4 side of the N (nitriding) film 10 by hot electron impregnation on the occasion of writing. Moreover, the electron by which the trap was carried out to the drain 4 by impressing a comparatively high electrical potential difference was read at the time of read-out. However, if high tension is impressed to a drain 4, as shown in drawing 9 B, a depletion layer 100 will be formed in the substrate 1 of the drain 4 circumference.
[0007] This depletion layer 100 spreads, and if an electron reaches even the part by which the trap is carried out, in spite of not forming the channel actually, it will be in the same condition as the case where a channel is formed. That is, since a channel will be formed even when the trap of the electron is carried out to the N (nitriding) film 10 and a channel originally is not formed, it will be detected if "1" is not written in. When conventional equipment was used, it was impossible thus, for a depletion layer 100 to perform breadth and exact read-out at the time of read-out.
[0008] Then, this invention aims at offer of the semiconductor device which can perform exact read-out.
[0009]
[Means for Solving the Problem] The semiconductor device concerning claim 1 is formed in the source field prepared in

the substrate, and a substrate. The trap film which was prepared so that the field which can be cable run formed might be formed a source field and in between and which was prepared on [which can be drain field cable run formed] the field, It is characterized by having the side conductive layer which insulated with the field which can be cable run formed, was prepared on [by the side of the control electrode prepared on the trap film, and the source / which can be cable run formed] the field, insulated with the control electrode on the side face of a control electrode, and was prepared in it.

[0010]

[Function] In the semiconductor device concerning this invention, a side conductive layer insulates with the field which can be cable run formed on [by the side of the source / which can be cable run formed] a field, and it insulates with a control electrode on the side face of a control electrode, and is prepared in it.

[0011] Therefore, since it is writing in by the source side, a source side is not reached, even if high tension is impressed to a drain side and a depletion layer spreads.

[0012]

[Example] One example of the trap mold semiconductor memory concerning this invention is hung up over drawing 2 B, and the structure is explained. In the P type substrate 1, the drain 4 as the source 2 which is a source field, and a drain field is formed, and the first oxide film 8, the N (nitriding) film 10, and the second oxide film 12 as trap film are formed on the substrate 1 (let three layer membranes of this first oxide film 8, the N (nitriding) film 10, and the second oxide film 12 be the ONO film 30 below). The oxide film 16 is formed so that the control gate 14 which is a control electrode may be formed on this ONO film 30 and the control gate 14 and a substrate 1 may be covered. The selector gate 20 as a side conductive layer is formed in the side face of the control gate 14, and the interlayer film 18 is also formed so that the control gate 14 and a substrate 1 may be covered. Furthermore, the bit line (drain wire) 25 is formed on the interlayer film 18.

[0013] Next, the outline of the trap mold semiconductor memory shown in drawing 2 B of operation is explained using drawing 1 . The operating state at the time of writing is hung up over drawing 1 A. In the trap mold semiconductor memory concerning this example, it is impressing high tension to a drain 4 side and the control gate 14, and impressing 0V to the source 2, and an electron elutriates of the source 2 to a drain 4, and the channel 80 as a field which can be cable run formed is formed between the source 2 and a drain 4. Here, the electrical potential difference of extent from which a substrate 1 will be in ON condition exactly is impressed to the selector gate 20 prepared in the source 2 side. By impressing such an electrical potential difference, electric field concentrate between a substrate 1 and a selector gate 20. The electron which elutriated of the source 2 serves as a hot electron by the electric field currently concentrated. Since high tension is impressed to the control gate at this time, the trap of some hot electrons is carried out to the source side of the N (nitriding) film 10 in the ONO film. The condition that the trap of this electron was carried out to the N (nitriding) film 10 is in the condition that "1" was written in.

[0014] The case where the electron by which the trap was carried out to the N (nitriding) film 10 is read is hung up, and drawing 1 B is explained. As mentioned above, the trap of the electron is carried out to the source 2 side of the N (nitriding) film 10. Therefore, even if it impresses a high electrical potential difference to a drain 4 in the case of read-out, a depletion layer does not reach the part where the trap of the electron is carried out. That is, as shown in drawing 1 B, even if a depletion layer 100 spreads near the drain 4, it becomes possible not to spread even in the source side of the N (nitriding) film 10, and to detect to accuracy whether it is that the trap of the electron is carried out to the N (nitriding) film 10 ("1" is written in). In addition, elimination is performed by emitting the electron by which the trap was carried out to a substrate 1.

[0015] Next, it explains using the equal circuit which shows the detail of the trap mold semiconductor memory of this example of operation to drawing 8 . Here, use a cel C10 as the selection cel which performs writing, elimination, and read-out for information, and let other cels (cels C20, C30, and C40) be non-choosing cels (drawing 8 A). The electrical potential difference impressed to each line, train, and part in each actuation event at drawing 8 B is shown.

[0016] First, in the case of informational writing, 9V are impressed to 10V and the bit line BL1, 1.5V are impressed to a pan at the selector-gate line SG1, and 0V are impressed to the control gate line CG 1 at others. At this time, in the selection cel C10, it is that 9V are given to the bit line BL1, an electron elutriates of the source 2 between drains 4 as mentioned above, and a channel 80 is formed (refer to drawing 1 A). Moreover, electric field concentrate between a substrate 1 and a selector gate 20 by the electrical potential difference from which a substrate called 1.5V is turned on exactly being impressed to a selector gate. The electron which elutriated of the source 2 by this concentrated electric field serves as a hot electron. Furthermore, since high tension called 10V in the 14 control gates is given to the control gate 14, the trap of some hot electrons is carried out to the source side of the N (nitriding) film 10 in the ONO film. In this way, the trap of some hot electrons ("1" is written in) is carried out to the N (nitriding) film 10.

[0017] In this way, if "1" is written in, the threshold of an electrical potential difference required for making the channel 80 shown in drawing 1 A form will rise. By detecting lifting of this threshold, it detects that "1" was written in. That is, a sense electrical potential difference is impressed to the control gate 14 as mentioned above, and if a channel is not formed between the source 2 and the gate 4 and a current does not flow, it detects that "1" was written in.
[0018] Here, if the non-choosing cel C20 is seen, 1.5V are given through 10V and the selector-gate line CG 1 through the control gate line SG1. However, since 0V which are the source 2 and this potential are given to the bit line BL2 and a channel is not formed, there is no possibility that incorrect writing may arise. Moreover, since 0V are respectively given to the selector-gate line SG2 and the control gate line CG 2 also about other non-choosing cels C30 and C40, there is no possibility that an incorrect store may arise in cels other than selection cel C10.
[0019] Next, the case where the electron by which the trap was carried out to the N (nitriding) film 10 is eliminated is explained. In this case, -15V are impressed to the control gate lines CG1 and CG2, respectively, both bit lines BL1 and BL2 are made open, and 0V are given to others. By impressing a negative electrical potential difference to the control gate, the electric field of the store and reverse which were mentioned above arise. Therefore, the electron by which the trap is carried out is pulled out and emitted to a substrate 1 by FN (Fowler-Norheim) tunneling. In this way, if the electron by which the trap was carried out is pulled out, the threshold of an electrical potential difference required for making the channel 80 shown in drawing 1 A form will descend. By detecting descent of this threshold, it is detected that information"1" is not written in from the N (nitriding) film 10. That is, if a sense electrical potential difference is impressed, a channel 80 is formed between the source 2 and a drain 4 as mentioned above and a current flows, it will be detected that information"1" is not written in from the N (nitriding) film 10.
[0020] Furthermore, read-out of the information from the selection cel C10 is explained. When reading the information memorized by the selection cel C10, 3V are given to the control gate line CG 1 as a sense electrical potential difference, in order to make a selector gate turn on, 5V are impressed to the selector-gate line SG1, and 2V are impressed to the bit line BL1. Here, a sense electrical potential difference is the mean value of a threshold in case the trap of the electron is carried out to the N (nitriding) film 10, and a threshold in case a trap is not carried out. Moreover, 0V are impressed in addition to the above.
[0021] If the selection cel C10 is in a write-in condition, a channel 80 (refer to drawing 1 A) will not be formed, and a current will not flow between the source and a drain. Therefore, in the sense amplifier (not shown) linked to the bit line BL1, a current cannot be detected but it reads that the selection cel C10 is in a write-in condition. On the other hand, if the selection cel C10 is in the condition of not writing in, the above-mentioned channel 80 will be formed between source drains. Therefore, a current flows between the source and a drain and it reads that the selection cel C10 is in the condition of not writing in by detecting this electrical potential difference with said sense amplifier.
[0022] Next, if it sees about the selection cel C20, 3V which are a sense electrical potential difference are impressed to the control gate line CG 1, and 5V are impressed to the selector-gate line SG1. However, since 0V are impressed to the bit line BL2 and it connects with the sense amplifier bit line BL1, read-out is not performed in the non-choosing cel C20. Furthermore, in other non-choosing cels C30 and C40, since 0V are given to the control gate line CG 2 and the selector-gate line SG2, respectively, read-out is not performed.
[0023] In this way, it becomes possible to perform informational writing on the N (nitriding) film 10 by the side of the source by the hot electron impregnation method, and to perform exact read-out by eliminating by FN tunneling.
[0024] The structure and the manufacture approach of trap mold memory concerning this example are explained below based on drawing. First, the manufacture approach of the trap mold memory shown in drawing 2 B is explained. The O film 8 is formed for a start by thermal oxidation on a substrate 1 (P well). Next, for a start, on the O film 8, LPCVD is used and N (nitriding) film 10 film is formed. next, the N (nitriding) film 10 top -- wet oxidation -- the -- 2O film 12 is formed (drawing 3 A). In this way, the first polish recon film 13 is formed on the formed ONO film 30 (drawing 3 A). Next, the control gate 14 is formed by etching the first polish recon film 13 like drawing 3 B. In order to form this control gate 14, in case the first polish recon film 13 is etched, an oxide film 16 is formed by thermal oxidation to the ONO film 30 and the control gate 1 which remove ONO film 30 other than under the control gate 14 and which were formed on the substrate 1 in this way (drawing 3 C) so that these may be covered (drawing 3 D). Next, the second polish recon film 28 is formed on an oxide film 16 (drawing 4 A). Etchback of this second polish recon film 28 is carried out by reactive etching (RIE) which is anisotropic etching, and sidewalls 20 and 22 are formed (drawing 4 B). Next, the ion implantation of the As (arsenic) is carried out to a substrate 1 by using sidewalls 20 and 22 and the control gate 14 as a mask (drawing 4 B). Etching removes only a sidewall 22 after As (arsenic) impregnation, and the ion implantation of the phosphorus is shortly carried out to a substrate by using a sidewall 20 and the control gate as a mask (drawing 4 C).
[0025] At this time, As (arsenic) and phosphorus which have already been driven into the substrate will overlap and

exist in almost all parts. However, only phosphorus exists in the substrate part BS 1 of a part with a sidewall 22 (drawing 5 A). After phosphorus is poured in, the BPSG film is formed as an interlayer film 18 (drawing 5 B). This BPSG is PSG (Phosoho-Silicate-Glass) which added boron. Next, a reflow of the interlayer film 18 is carried out. Thermal diffusion of As (arsenic) and phosphorus which were driven in in the substrate 1 on the occasion of this reflow is carried out, and as shown in drawing 5 B, the drain 4 of the source 2 and LDD (Lightly-Doped-Drain) structure is formed. That is, the substrate part BS 1 into which only the phosphorus by the side of a drain is driven has thin concentration compared with As (arsenic) and the part into which phosphorus was driven, and it becomes n-, and other parts become n+ and serve as LDD structure. This LDD structure is structure which eases about four-drain electric field.

[0026] As mentioned above, after forming the source 2 and a drain 4, while DEPOSHISHON and carrying out patterning of the aluminum (aluminum) and forming the bit line (drain wire) 25 on the layer intermediate layer 18, the passivation film (not shown) is also formed on the bit line 25 (drawing 2 B). Thus, the trap mold semiconductor memory shown in drawing 2 B is manufactured.

[0027] Next, the structure of other examples of the trap mold semiconductor memory concerning this invention is hung up over drawing 2 A. Compared with the thing of the above-mentioned drawing 2 B, the memory of drawing 2 A differs in that the ONO film 30 is formed the whole surface on a substrate 1. However, both operate as memory by performing same actuation. The manufacture approach of drawing 2 A is explained below.

[0028] It is the same as that of the above-mentioned process until it generates the ONO film 30, it forms the first polish recon film 13 on the ONO film 30 and it forms the control gate 14 by etching on a substrate 1 (refer to the drawing 3 A, drawing 6 A). However, unlike the above-mentioned manufacture approach, the ONO film 30 is not etched but an oxide film 16 is formed on the ONO film 30 and a substrate 1 by thermal oxidation (drawing 6 A). Since the subsequent process is the same as the manufacture approach of the trap mold semiconductor memory of the above-mentioned drawing 2 B, it explains briefly.

[0029] The second polish recon film 28 is formed on the formed oxide film 16 (drawing 6 B). Etchback of this second polish recon film 28 is carried out by reactive etching (RIE) which is anisotropic etching, and sidewalls 20 and 22 are formed (drawing 6 C). Next, As (arsenic) is driven in to a substrate 1 by using sidewalls 20 and 22 and the control gate 14 as a mask (drawing 6 C).

[0030] After driving in As (arsenic), etching removes only a sidewall 22 (drawing 7 A). Furthermore, phosphorus is driven in to a substrate 1 by using a sidewall 20 and the control gate 14 as a mask (drawing 7 B). After driving in phosphorus, the BPSG film is formed as an interlayer film 18 (drawing 7 B). Thermal diffusion of As (arsenic) and phosphorus which were driven in at the time of the reflow of this BPSG film is carried out, and the source 2 and a drain 4 are formed (drawing 7 C). Also in the case of this diffusion, a drain 4 side serves as LDD structure as mentioned above according to the concentration difference of the part into which the part, the phosphorus, and the arsenic of only phosphorus were driven.

[0031] After the source 2 and drain 4 formation, while DEPOSHISHON and carrying out patterning of the aluminum (aluminum) and forming the bit line (drain wire) 25 on an interlayer film 18, the passivation film (not shown) is formed on the bit line 25 (drawing 2 A). Thus, the trap mold semiconductor memory shown in drawing 2 A is manufactured.

[0032]

[Effect of the Invention] In the semiconductor device concerning this invention, a side conductive layer insulates with the field which can be cable run formed on [by the side of the source / which can be cable run formed] a field, and it insulates with a control electrode on the side face of a control electrode, and is prepared in it. That is, since it is writing in by the source side, a source side is not reached, even if high tension is impressed to a drain side and a depletion layer spreads.

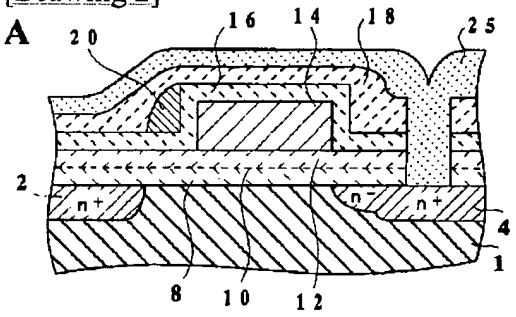
[0033] Therefore, it becomes possible to perform exact reading.

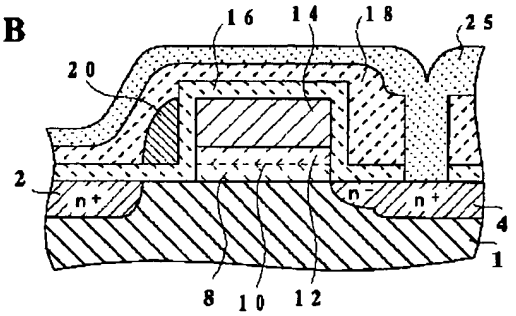
[Translation done.]

* NOTICES *

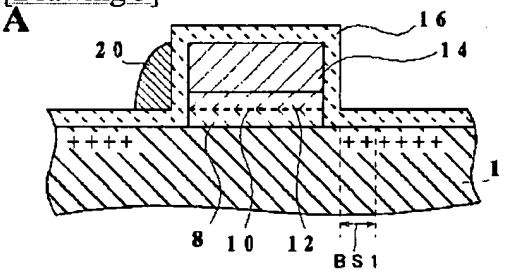
DRAWINGS

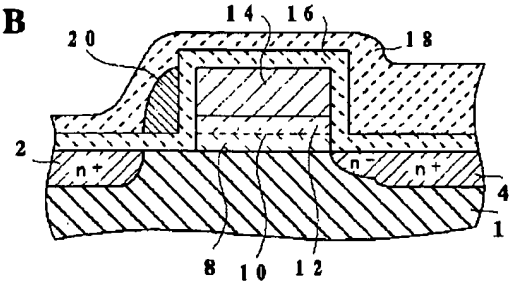
[Drawing 2]



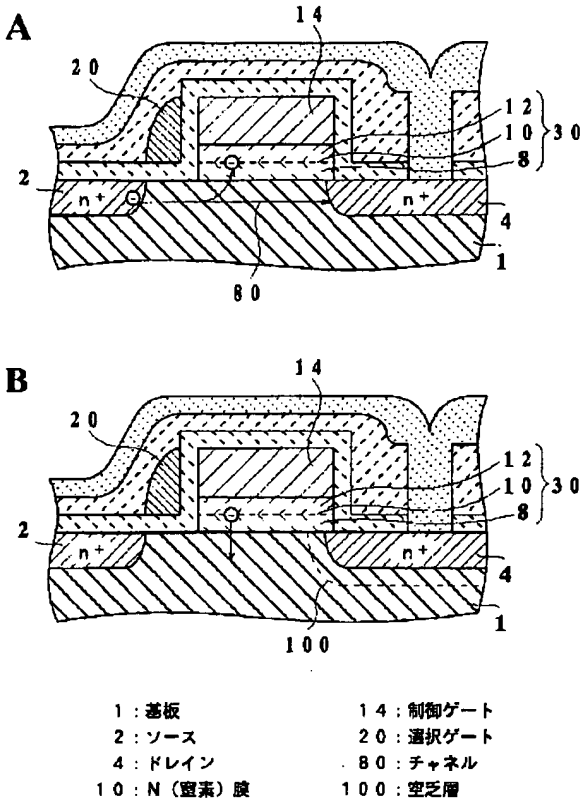


[Drawing 5]



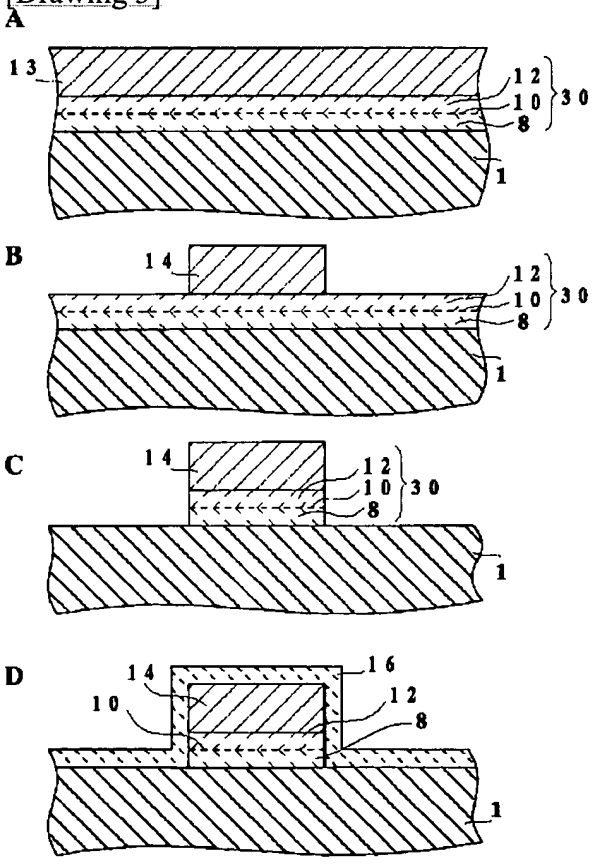


[Drawing 1]

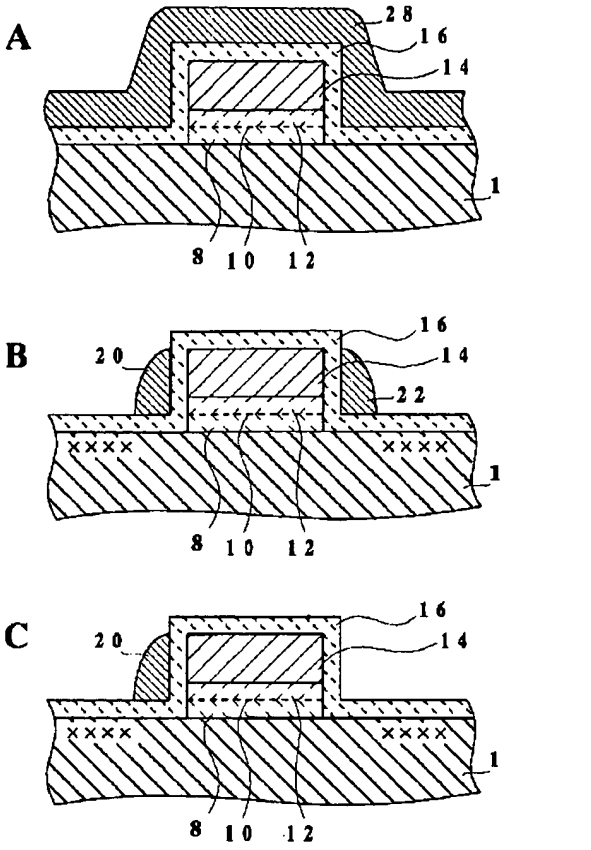


1：基板　14：制御ゲート
2：ソース　20：選択ゲート
4：ドレイン　80：チャネル
10：N（窒素）膜　100：空乏層

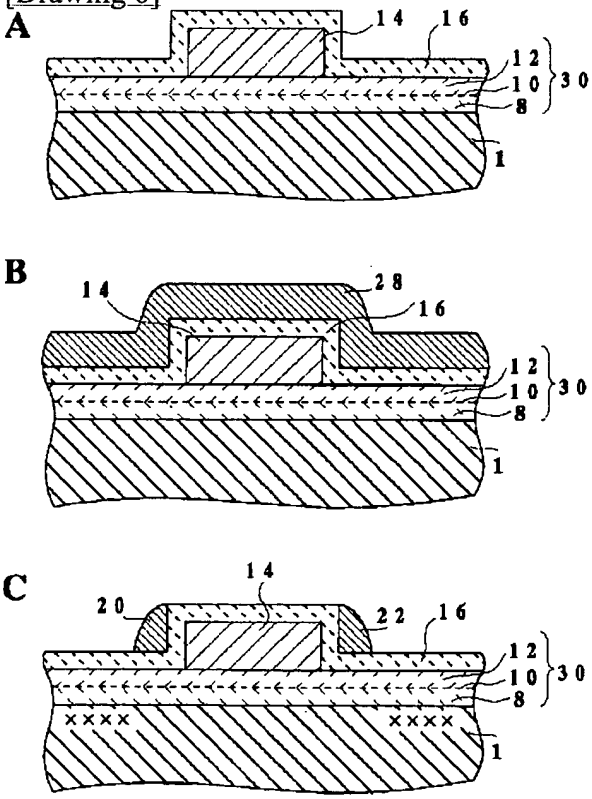
[Drawing 3]



[Drawing 4]



[Drawing 6]



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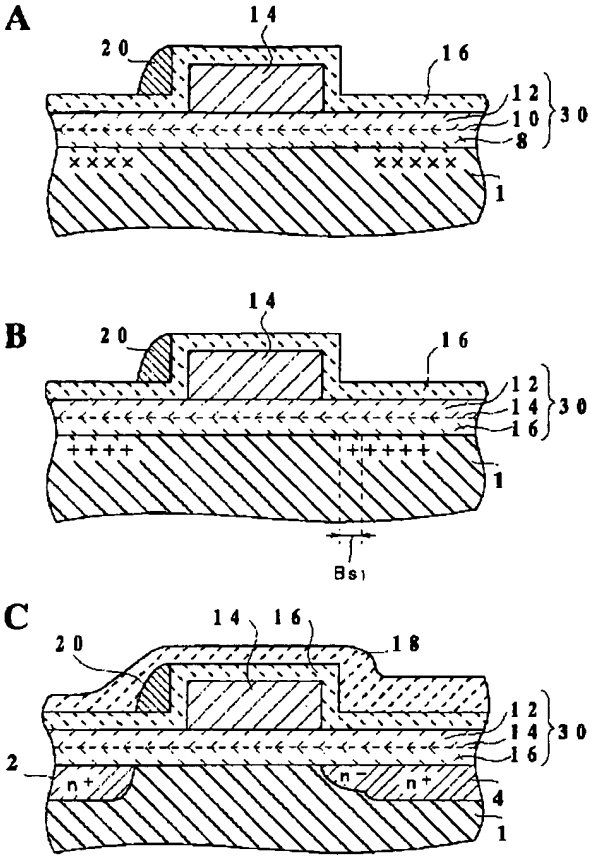

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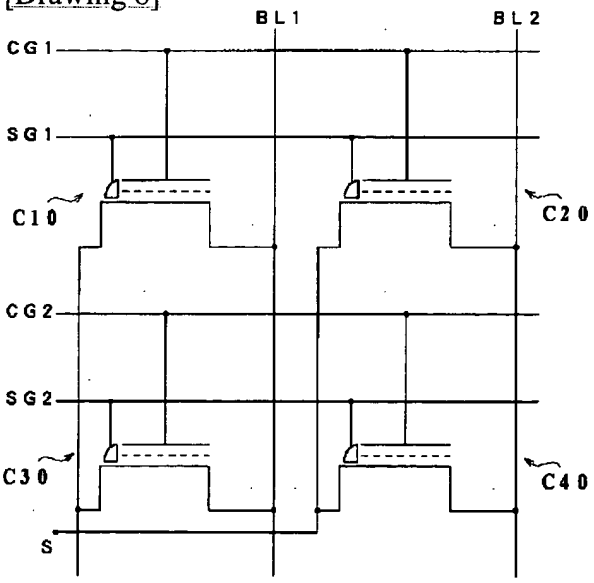
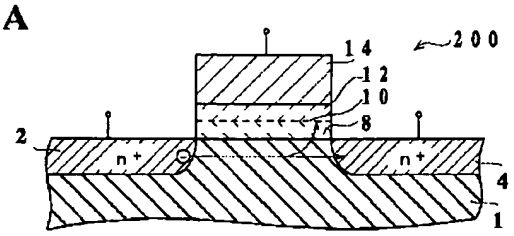


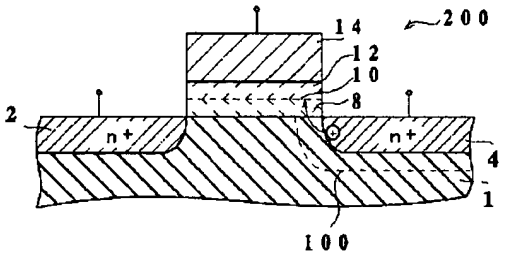
(V)	CG1	CG2	SG1	SG2	BL1	BL2	S	SUB
書込み	10	0	1.5	0	9	0	0	0
消去	-15	-15	0	0	OPEN	OPEN	0	0
読み出し	3	0	5	0	2	0	0	0

[Drawing 9]

A



B



[Translation done.]